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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/759,414	01/13/2001	Zhe Li		2309

7590 06/03/2004

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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/759,414	LI, ZHE	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/13/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are examined.

Drawings

2. Figures 2 and 4 are common electrical devices and should be labeled as prior art.

Priority

3. Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged from provision application number 60/176,446 on 1/14/2000.

Claim Interpretation

4. Office personnel are to give claims their **"broadest reasonable interpretation"** in light of the supporting disclosure. *In re Morris,* 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater,* 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551(CCPA 1969). See *also *In re Zletz,* 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322(Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow") .... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed .... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process. The examiner

interprets the claims as a process to reduce chip design implementation for a reduced equivalent circuit.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

6. Regarding claims 1,8, 9,11-13, and 15 state the phrase "such that" which renders the claims indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

7. Furthermore, claims 6-8,14 and 15 state the phrase "likelihood" which renders the claims indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Puri et al. (U.S. Patent 5,469, 367 (1995)).

Puri et al. teaches a machine methodology for designing asynchronous circuits using a modular approach for the synthesis of asynchronous circuits from signal transition (abstract).

Claim 1. A method for debugging a circuit design with constraining information, the constraining information including a first set of at least one candidate branch, a second set of at least one correction probe, and a third set of at least zero restriction probe, comprising the steps of (column 4, lines 3-14 and 27-34): building a representation of the relationships among objects including said circuit design, said first set of at least one candidate branch, said second set of at least one correction probe, and said third set of at least zero restriction probe; and identifying combinations of behaviors at members of said first set of at least one candidate branch such that said circuit design satisfies the expectation expressed in said second set of at least one correction probe and said third set of at least zero restriction probe (column 22, lines 57-65, figure 9, (402,404)).

Claim 2. The method of claim 1, wherein said representation of the relationships among objects including said circuit design, said first set of at least one candidate branch, said second set of at least one correction probe, and said third set of at least zero restriction probe is a fourth set of at least one binary decision diagram (column 4, lines 24-34).

Claim 3. The method of claim 2, wherein an input variable of a member of said fourth set of at least one binary decision diagram corresponds to a member of said first set of at least one candidate branch(column 4, lines 24-34).

Claim 4.The method of claim 3, wherein said combinations of behaviors at members of said first set of at least one candidate branch such that said circuit design satisfies the expectation expressed (column, 22, lines 35-38) in said second set of at least one correction probe and said third set of at least zero restriction probe are represented as paths that connect the root node to a predetermined leaf node in a member of said fourth set of at least one binary decision diagram (column 22, lines 27-51).

Claim 5. The method of claim 4, wherein a member of said fourth set of at least one binary decision diagram is ordered and reduced(column 22, lines 27-51).

Claim 6.The method of claim 5, wherein further comprising the step of: computing, based on said combinations of behaviors at members of said first set of at least one candidate branch, a likelihood rating for a member of said first set of at least one candidate branch (column 22, lines 27-51).

Claim 7.The method of claim 6, wherein further comprising the step of: determining, based on said likelihood rating for said member of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch must be changed such that said circuit design satisfies the expectation expressed in said second set of at least one correction probe and said third set of at least zero restriction probe(column 22, lines 27-51).

Claim 8. The method of claim 6, wherein further comprising the step of: determining, based on said likelihood rating for said member of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch can be changed, in association with changes of behaviors at other members of said first set of at least one candidate branch, such that said circuit design satisfies the expectation (column, 22, lines 35-38) expressed in said second set of at least one correction probe and said third set of at least zero restriction probe (column 22, lines 27-51).

Claim 9.The method of claim 6, wherein further comprising the step of: of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch is never required to be changed such that said circuit design satisfies (column, 22, lines 35-38) the expectation expressed in said second set of at least one correction probe and said third set of at least zero restriction probe (column 22, lines 27-51).

Claim 10. The method of claim 5, wherein further comprising the step of: determining, based on said combinations of behaviors at members of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch has no impact on whether said circuit design satisfies the expectation (column 22, lines 38-41) expressed in said second set of at least one correction probe and said third set of at least zero restriction probe (column 22, lines 27-51).

Claim 11.The method of claim 5, wherein further comprising the step of: 8. The method of claim 6, wherein further comprising the step of: determining, based on said likelihood rating for said member of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch can be changed, in association with changes of behaviors at other members of said first set of at least one candidate branch, such that said circuit design satisfies the expectation (column 22, lines 41-43) expressed in said second set of at least one correction probe and said third set of at least zero restriction probe (column 22, lines 27-51).

Claim 12. The method of claim 4, wherein further comprising the step of: determining, based on said combinations of behaviors at members of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch can be changed, in association with changes of behaviors at other members of said first set of at least one candidate branch, such that said circuit design

satisfies the expectation expressed in said send set of at least one correction probe and said third set of at least zero restriction probe(column 22, lines 27-51).

Claim 13. The method of claim 1, wherein further comprising the step of: determining, based on said combinations of behaviors at members of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch can be changed, in association with changes of behaviors at other members of said first set of at least one candidate branch, such that said circuit design satisfies the expectation expressed in said (column 22, lines 27-51).

Claim 14. The method of claim 1, wherein further comprising the step of: computing a likelihood rating for a member of said first set of at least one candidate branch based on said combinations of behaviors at members of said first set of at least one candidate branch(column 22, lines 27-51).

Claim 15. The method of claim 14, wherein further comprising the step of: determining, based on said likelihood rating for said member of said first set of at least one candidate branch, whether the behavior at said member of said first set of at least one candidate branch can be changed, in association with changes of behaviors at other members of said first set of at least one candidate branch, such that said circuit design satisfies the expectation (column 22, lines 34-43) expressed in said second set of at least one correction probe and said third set of at least zero restriction probe (columns 27, 28: claims 1 and 3).

Claim 16. The method of claim 1, wherein further comprising the step of: constructing a fifth set of at least one branch cone wherein each input to a member of said fifth set of at least one branch cone corresponds to a member of said first set of at least one candidate branch, whereby said fifth set of at least one branch cone is used for the step of building said representation of the relationships among objects including said circuit design, said first set of at least one candidate branch, said second set of at least one correction probe, and said third set of at least zero restriction probe (columns 27, 28: claims 1 and 3).

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom Stevens whose telephone number is (703) 305-0365, Monday-Friday (8:30 am- 5:30 pm) or contact Supervisor Mr. Kevin Teska at (703) 305-9704. The fax number for the group is 703-872-9306.

Any inquires of general nature or relating to the status of this application should be directed to the Group receptionist whose phone number is (703) 305-3900.

May 21, 2004

THS